

**General Description**

The DMA controller can be used to transfer a memory block from one memory location to another. Currently it supports only word (= 32 bit) transfers.

The bit `enblae_dma_done_irq` of the CONTROL register allows to issue an interrupt after DMA transfer is finished.

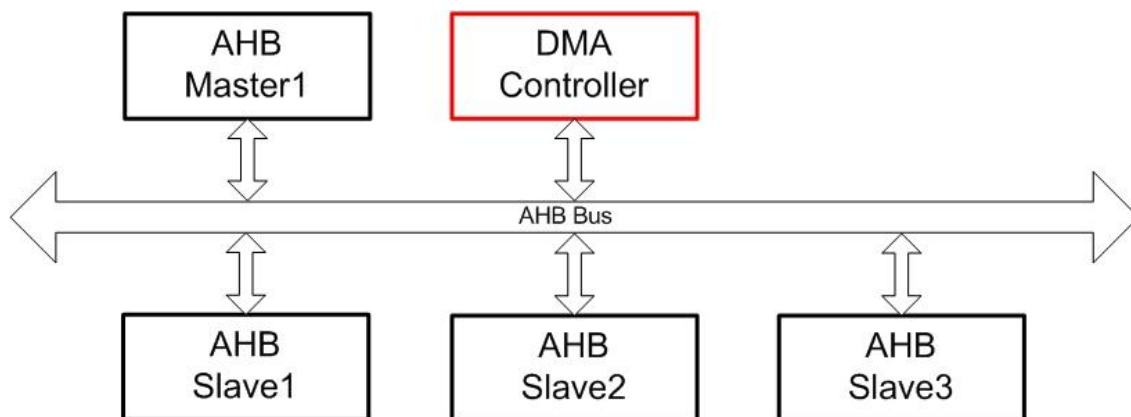
**Features**

The DMA controller allows transferring a data blocks from one memory location to another.

- Implemented as AHB master
- Programmable Transfer Size
- Optional Interrupt after Data Transfer
- Source Address Increment: either +1 Word or No Increment
- Destination Address Increment: either +1 Word or No Increment

Manual: GERA-DMA Manual V1.0.pdf

**Block Diagram**



**Device Utilization & Performance**

Technology	Device	Utilization <small>(Average out of some different applications)</small>	Performance
Stratix III (Altera)	EP3SL150F780	Logic Elements: 760 Block Memory: 0	100 MHz AHB bus clock
ArriaGX (Altera)	EP1AGX90EF1	Logic Elements: 760 Block Memory: 0	100 MHz AHB bus clock