

General Description

The availability of Gigabit line interfaces not only requires faster input/output within a system (e.g. DMA) but also puts additional burden on software within operating systems to process the protocol layers at higher speed. The higher bandwidth results in higher CPU load to process the traffic which reduces the overall system performance or creates higher cost caused by the need for more processing power.

On the other hand within embedded systems CPU resources are often limited and even serving a 100Mbit/s network can be out of reach for these applications. To address these bottlenecks, the Ethernet MAC-NET Core implements, in addition to Layer 2 Ethernet MAC functions, Layer 3&4 network protocol acceleration functions. It is designed to accelerate the processing of various common networking protocols such as IPv4/v6, TCP, UDP and ICMP providing wire speed services to client applications.

To complement the MAC Core, flexible interface options (e.g. GMII/MII, RGMII, SGMII) and physical layer (PCS) Cores are available addressing system needs and enabling seamless interconnect to any standard PHY device. The MAC Core can be implemented in FPGA and ASIC.

The MAC Core is fully UNH certified and is interoperable with major PHY vendor and systems.

Features

- Implements the full 802.3 specification with preamble / SFD generation, frame padding generation, CRC generation and checking
- Dynamically configurable to support 10Mbps, 100Mbps or 1Gbps operation
- Supports full duplex and optionally 10/100 half-duplex
- Support for AMD Magic Packet detection with interrupt for node remote power management
- Standard PHY interface with 8-Bit Gigabit Medium Independent Interface (GMII) operating at 125MHz and 4-Bit MII operating at 25MHz
- 32-bit AMBA 3 AHB-Lite (v1.0) system interface with burst support for efficient frame transactions
- Integrated 32-bit FIFOs with programmable threshold settings enabling store&forward operation allowing for fully independent AHB system clock
- CRC-32 checking and generation with optional forwarding to/from user application
- Implements fully automated Pause Frame (802.3 Annex 31A) generation with programmable quanta and termination providing automated flow control
- Support for IEEE 802.1q VLAN tagged frames
- Flexible MAC address filtering, promiscuous mode support and automatic address insertion on transmit Programmable frame maximum length providing support for any standard or proprietary frame length up to 16K
- Statistics for IEEE 802.3 Management Information Database (MIB) package, Ethernet MIB (RFC 2665) and Remote Network Monitoring (RFC 2819)
- MDIO Master interface for PHY device management
- Automatic IP-header and payload (protocol specific) checksum calculation with verification on receive and insertion on transmit
- Support for IP and TCP, UDP, ICMP data for checksum generation and checking
- IPv4 and IPv6 support with transparent passing of frames of other types and protocols
- Checksum calculation with full header options support for IPv4 and TCP protocol headers
- IPv6 support limited to datagrams with base header. Frames with extension headers passed transparently.
- Configurable Ethernet Payload alignment to allow for 32-bit word aligned IP header and data processing

Functional Description

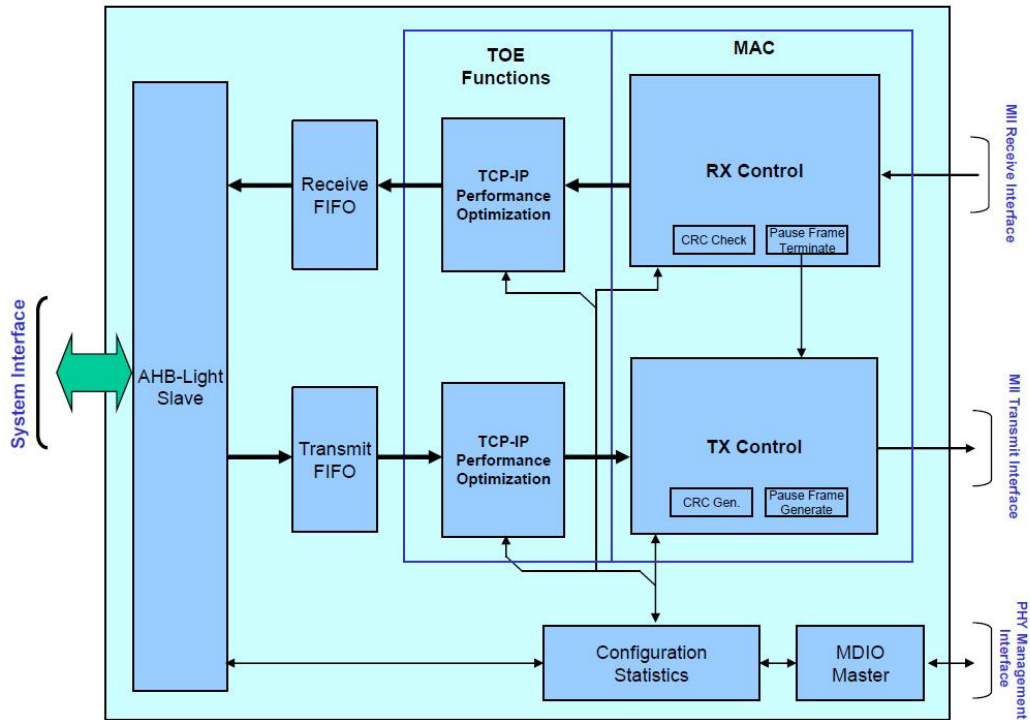
The core includes a 32-bit AMBA AHB system interface with burst support for efficient frame transactions.

The core can be handled with our AMBA- IP Manager or standalone.

The core can be delivered only as an encrypted netlist for Altera FPGAs, RTL netlist can be ordered directly from MorethanIP.

LINUX driver available!

Block Diagram



Device Utilisation & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
ARRIA (2) (Altera)	different	Logic Elements: 6187 Block Memory: 92576 bit	100 MHz AHB bus clock