

General Description

This Gleichmann Research IP-Core provides a programmable universal Timer / Counter / PWM. Different interrupt possibilities guarantee a big flexibility.

Manual GERA-TIM Manual V1.0.pdf

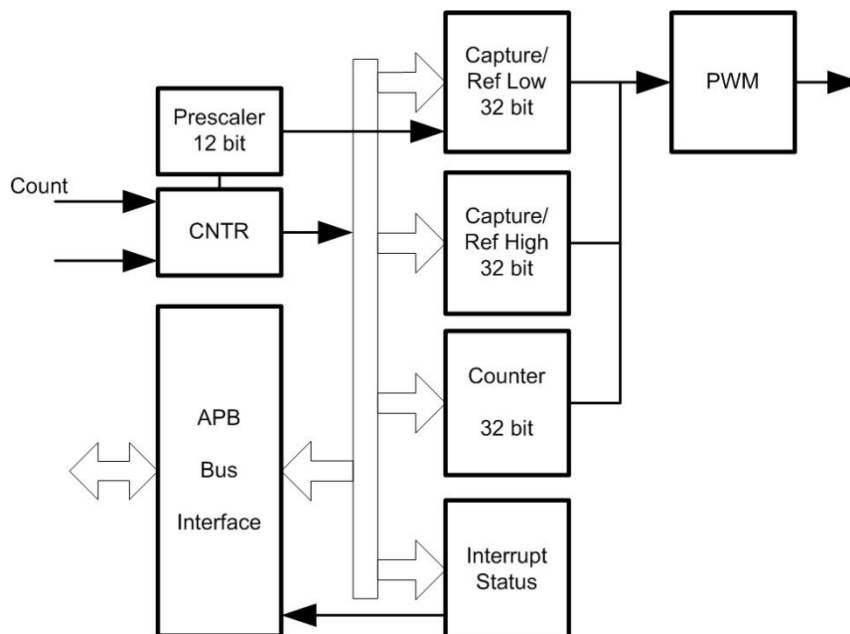
Features

- AMBA 3.0 APB interface
- 32-bit Single Channel Counter
- Single or Continuous Run
- External Event Counter
- Clock Gating
- PWM Signal Generator with Tri-State Driver Control Output
- High and Low Reference/Capture Registers
- Compare and Capture Interrupts
- 12-bit Clock Prescaler

Functional Description

The core has an AMBA APB bus communication interface and includes programmable registers that can be modified depending on the desired functionality of the IP-Core.

Block Diagram



Device Utilization & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
Stratix III (Altera)	EP3SL150F780C2	Logic Elements: 338 Block Memory: 0	100 MHz AHB bus clock
ArriaGX (Altera)	EP1AGX90EF1152C6	Logic Elements: 423 Block Memory: 0	100 MHz AHB bus clock