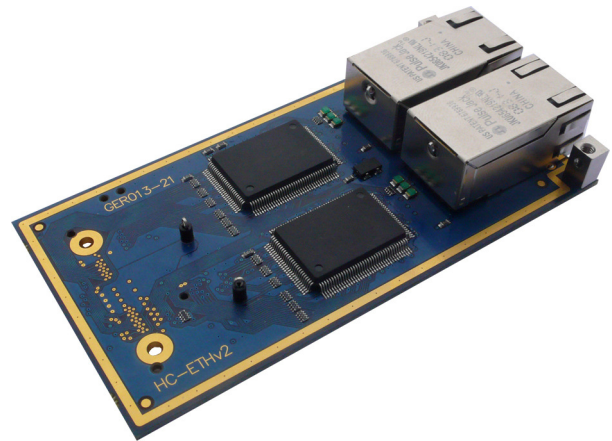


### 2 Ethernet Interfaces with 10/100 Mbit/s

Usable for Hpe\_midiv2 or Hpe\_IRP

#### General Description:

The Hpe\_childboard HC-ETHv2 offers two additional Ethernet connections for the Hpe system. Major component of each interface is the National **DP83865**. This chip fully features physical layer transceivers with integrated PMD sublayers to support 10BASE-T, 100BASE-TX and 1000BASE-T Ethernet protocols. The DP83865 is an ultra low power version of the DP83861 respectively the DP83891. Amongst others, it also features:

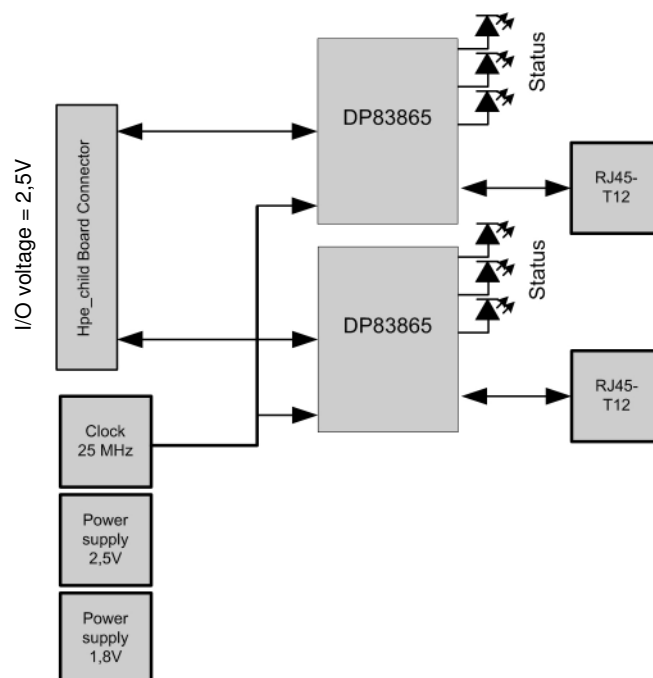


- LED support for activity, full/half duplex, link1000, link100 and link10, user programmable (manual on/off), or reduced LED mode
- IEEE 802.3u MII
- IEEE 802.3z GMII
- RGMII version 1.3
- User programmable GMII pin ordering
- IEEE 802.3u Auto-Negotiation and Parallel Detection
- Fully auto negotiates between 100 Mb/s, and 10 Mb/s full duplex and half duplex devices
- Speed ballback mode to achieve quality link

For more details refer to the datasheet of the DP83865.

(The module is not released for 1 Gbit use!)

#### Block Diagram:



**Pin description:**

A1	ETH0_GTX_CLK	A2	ETH0_CLK_TO_MAC	B1	ETH1_GTX_CLK	B2	ETH1_CLK_TO_MAC
A3	ETH0_RX_CLK	A4		B3	ETH1_RX_CLK	B4	
A5	GND	A6	GND	B5	GND	B6	GND
A7	ETH0_TXD0	A8	ETH0_RXD0	B7	ETH1_TXD0	B8	ETH1_RXD0
A9	ETH0_TXD1	A10	ETH0_RXD1	B9	ETH1_TXD1	B10	ETH1_RXD1
A11	ETH0_TXD2	A12	ETH0_RXD2	B11	ETH1_TXD2	B12	ETH1_RXD2
A13	ETH0_TXD3	A14	ETH0_RXD3	B13	ETH1_TXD3	B14	ETH1_RXD3
A15	ETH0_TXD4	A16	ETH0_RXD4	B15	ETH1_TXD4	B16	ETH1_RXD4
A17	ETH0_TXD5	A18	ETH0_RXD5	B17	ETH1_TXD5	B18	ETH1_RXD5
A19	ETH0_TXD6	A20	ETH0_RXD6	B19	ETH1_TXD6	B20	ETH1_RXD6
A21	ETH0_TXD7	A22	ETH0_RXD7	B21	ETH1_TXD7	B22	ETH1_RXD7
A23		A24		B23		B24	
A25		A26		B25		B26	
A27		A28		B27		B28	
A29	Vcc3V3	A30	GND	B29		B30	GND
A31	Vcc3V3	A32	GND	B31		B32	
A33	Vcc3V3	A34	GND	B33		B34	
A35	Vcc3V3	A36	GND	B35		B36	GND
A37	Vcc3V3	A38	GND	B37		B38	GND
A39	Vcc3V3	A40	GND	B39		B40	
A41	Vcc3V3	A42	GND	B41		B42	
A43	Vcc3V3	A44	GND	B43		B44	GND
A45	ETH0_TXER	A46	ETH0_RGMII_SELO	B45	ETH1_TXER	B46	ETH1_RGMII_SELO
A47	ETH0_TX_EN	A48	ETH0_RGMII_SEL1	B47	ETH1_TX_EN	B48	ETH1_RGMII_SEL1
A49	ETH0_RXER	A50	ETH0_AN_EN	B49	ETH1_RXER	B50	ETH1_AN_EN
A51	ETH0_RX_DV	A52	ETH0_MULT_EN	B51	ETH1_RX_DV	B52	ETH1_MULT_EN
A53	ETH0_COL	A54	ETH0_MDIX_EN	B53	ETH1_COL	B54	ETH1_MDIX_EN
A55	ETH0_DUPLEX	A56	ETH0_PHY0	B55	ETH1_DUPLEX	B56	ETH1_PHY0
A57	ETH0_SPEED0	A58	ETH0_PHY1	B57	ETH1_SPEED0	B58	ETH1_PHY1
A59	ETH0_SPEED1	A60	ETH0_PHY2	B59	ETH1_SPEED1	B60	ETH1_PHY2
A61	ETH0_MDC	A62	ETH0_PHY3	B61	ETH1_MDC	B62	ETH1_PHY3
A63	ETH0_MDIO	A64	ETH0_PHY4	B63	ETH1_MDIO	B64	ETH1_PHY4
A65	ETH0_MDINTR	A66	ETH_RES	B65	ETH1_MDINTR	B66	

Remark: The pins without any name are still driven from the main board with signals, Vdd or GND. Which signal levels or types, please refer to the manual of the base board.

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