

HC-SDRv2

SDRAM Memory Board

Usable for Hpe_midiv2 or Hpe_IRP

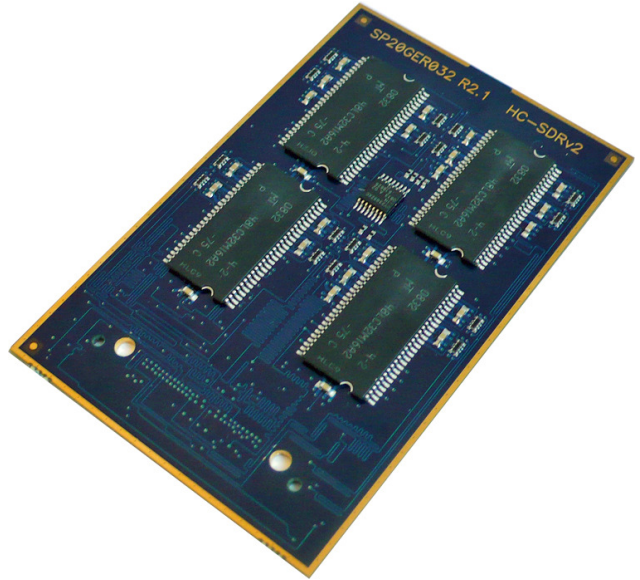
General Description:

The HC-SDRv2 is a standard child board.

The module is organized 32M * 64bit.

The SDRAM module can be used for graphic and video applications where you need a SDRAM directly connected to the internal controller (independent from the CPU memory bus).

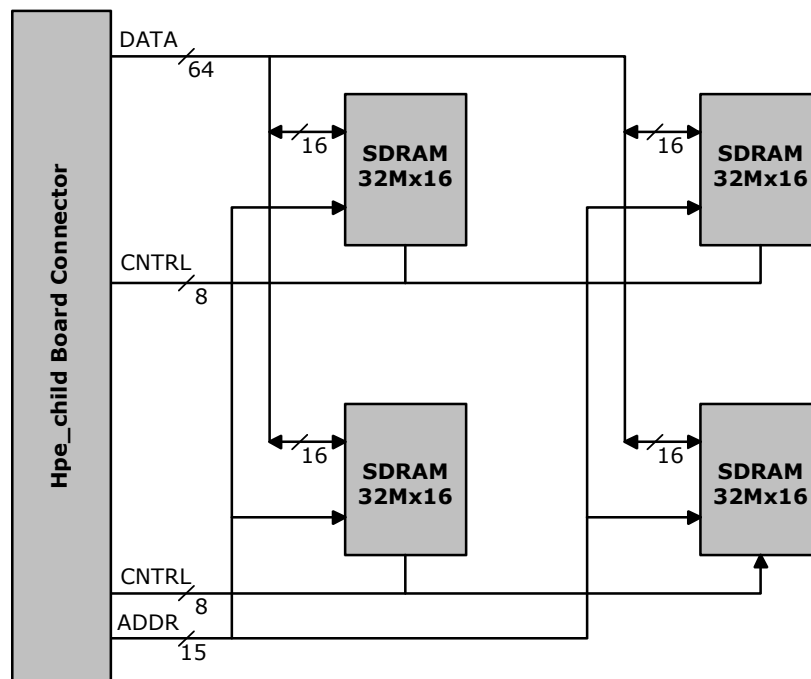
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh mode
- 64ms, 8,192-cycle refresh
- **120MHz** clock frequency



For more details refer to the datasheet of the MTC48LC32M16A2P-75.

- Constraints file on demand.

Block Diagram:



Pin description:

A1	SDR_CLK	A2	SDR_FBCLK	B1	SDR_RAS#	B2	SDR_CKE
A3	SDR_ZDB S1	A4	SDR_ZDB S2	B3	SDR_CAS#	B4	SDR_CS#
A5	GND	A6	GND	B5	GND	B6	GND
A7	SDR_DQ0	A8	SDR_DQ1	B7	SDR_DQ2	B8	SDR_DQ3
A9	SDR_DQ4	A10	SDR_DQ5	B9	SDR_DQ6	B10	SDR_DQ7
A11	SDR_DQ8	A12	SDR_DQ9	B11	SDR_DQ10	B12	SDR_DQ11
A13	SDR_DQ12	A14	SDR_DQ13	B13	SDR_DQ14	B14	SDR_DQ15
A15	SDR_DQ16	A16	SDR_DQ17	B15	SDR_DQ18	B16	SDR_DQ19
A17	SDR_DQ20	A18	SDR_DQ21	B17	SDR_DQ22	B18	SDR_DQ23
A19	SDR_DQ24	A20	SDR_DQ25	B19	SDR_DQ26	B20	SDR_DQ27
A21	SDR_DQ28	A22	SDR_DQ29	B21	SDR_DQ30	B22	SDR_DQ31
A23	SDR_DQ32	A24	SDR_DQ33	B23	SDR_DQ34	B24	SDR_DQ35
A25	SDR_DQ36	A26	SDR_DQ37	B25	SDR_DQ38	B26	SDR_DQ39
A27	SDR_DQ40	A28	SDR_DQ41	B27	SDR_DQ42	B28	SDR_DQ43
A29	VCC3V3	A30	GND	B29		B30	GND
A31	VCC3V3	A32	GND	B31		B32	SDR_BA0
A33	VCC3V3	A34	GND	B33		B34	SDR_BA1
A35	VCC3V3	A36	GND	B35		B36	GND
A37	VCC3V3	A38	GND	B37		B38	GND
A39	VCC3V3	A40	GND	B39		B40	SDR_WE#
A41	VCC3V3	A42	GND	B41		B42	
A43	VCC3V3	A44	GND	B43		B44	GND
A45	SDR_DQ44	A46	SDR_DQ45	B45	SDR_DQ46	B46	SDR_DQ47
A47	SDR_DQ48	A48	SDR_DQ49	B47	SDR_DQ50	B48	SDR_DQ51
A49	SDR_DQ52	A50	SDR_DQ53	B49	SDR_DQ54	B50	SDR_DQ55
A51	SDR_DQ56	A52	SDR_DQ57	B51	SDR_DQ58	B52	SDR_DQ59
A53	SDR_DQ60	A54	SDR_DQ61	B53	SDR_DQ62	B54	SDR_DQ63
A55	SDR_A0	A56	SDR_A1	B55	SDR_A2	B56	SDR_A3
A57	SDR_A4	A58	SDR_A5	B57	SDR_A6	B58	SDR_A7
A59	SDR_A8	A60	SDR_A9	B59	SDR_A10	B60	SDR_A11
A61	SDR_A12	A62		B61		B62	
A63	SDR_MDQ0	A64	SDR_MDQ1	B63	SDR_MDQ2	B64	SDR_MDQ3
A65	SDR_MDQ4	A66	SDR_MDQ5	B65	SDR_MDQ6	B66	SDR_MDQ7

Remark: The pins without any name are still driven from the main board with signals, Vdd or GND. Which signal levels or types, please refer to the manual of the base board.

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