

## General Description

This core is based on the Philips SJA1000 controller and has a compatible register map with a few exceptions. The SJA1000 is a stand-alone controller for the Controller Area Network (CAN).

Please download manual from the internet, e.g.  
[http://www.nxp.com/documents/data\\_sheet/SJA1000.pdf](http://www.nxp.com/documents/data_sheet/SJA1000.pdf)

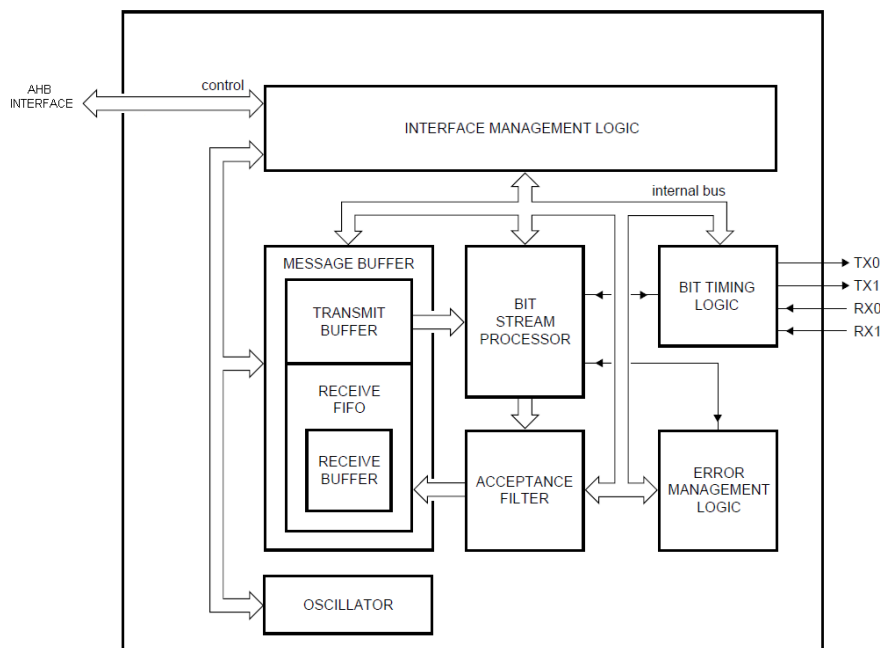
## Features

- AMBA 2.0 AHB interface
- CAN 2.0B protocol compatible
- BasicCAN mode; PCA82C200 compatible
- PeliCAN mode (with extended features)
- Configurable acceptance filter register
- Programmable Baud generator
- Bit rates up to 1 Mbits/s
- Extended receive buffer (64-byte FIFO)
- Supports 11-bit identifier as well as 29-bit identifier

## Functional Description

The core has an AMBA AHB bus communication interface and includes programmable registers that can be modified depending on the desired communication protocol and communication target. The clock divider register is used to select the CAN operation mode (BasicCAN/PeliCAN). The acceptance filter compares the received identifier with the acceptance filter register contents and decides whether this message should be accepted or not.

## Block Diagram



## Device Utilisation & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
Stratix III (Altera)	EP3SL150F780C2	Logic Elements: 1150 Block Memory: 832 bit	100 MHz AHB bus clock
ArriaGX (Altera)	EP1AGX90EF1152C6	Logic Elements: 1285 Block Memory: 832 bit	100 MHz AHB bus clock