

### General Description

The Ethernet core implements a dual speed 10/100Mbps Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with Full Duplex Ethernet LANs and legacy Half Duplex 10/100Mbps Ethernet and Fast Ethernet LANs.

The core is licensed from MorethanIP. This guarantees an excellent product status and quality.

Manual: 10\_100\_mac\_net\_ref\_guide\_v1.2.pdf

### Features

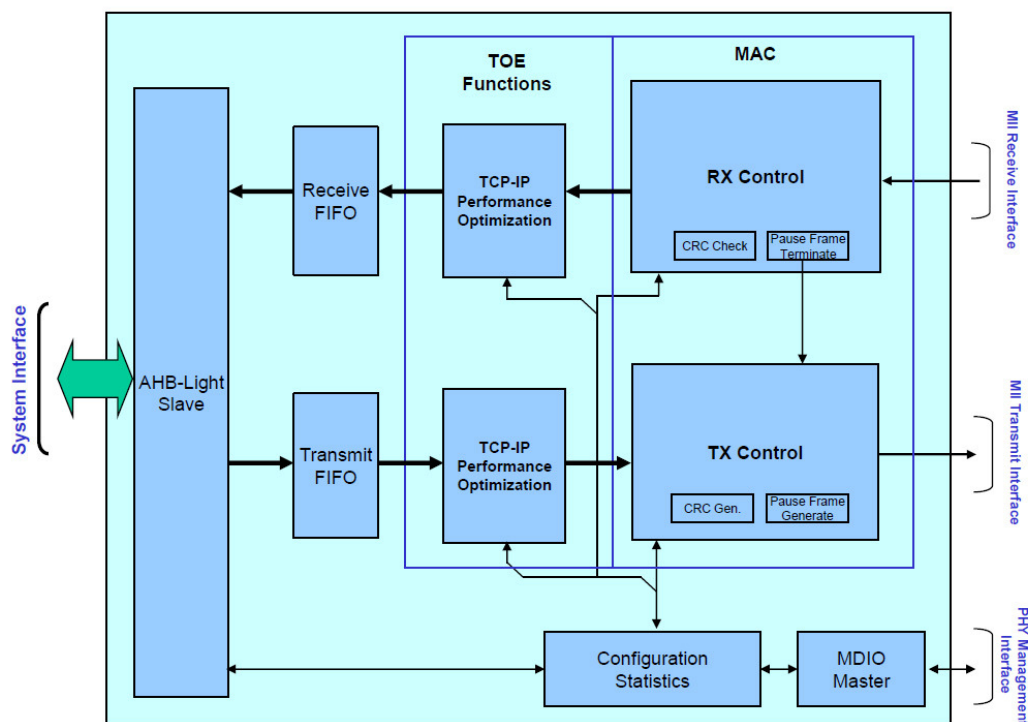
- Implements the full 802.3 specification with preamble /
- SFD generation, frame padding generation, CRC generation and checking
- Support 10Mbps and 100Mbps modes of operation
- Supports full duplex and optionally 10/100 half-duplex
- Standard PHY interface with 4-Bit MII operating at 25MHz

Please refer to the manual for more details.

### Functional Description

The Core includes a 32-bit AMBA 3 AHB system interface with burst support for efficient frame transactions. The MAC Core can be implemented in FPGA and ASIC. The MAC Core is fully UNH certified and is interoperable with all PHY vendor and systems.

### Block Diagram



### Device Utilisation & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
Stratix III (Altera)	EP3SL150F780C2	Logic Elements: 6081 Block Memory: 85.248 bit	100 MHz AHB bus clock
ArriaGX (Altera)	EP1AGX90EF1152C6	Logic Elements: 5662 Block Memory: 92.576 bit	100 MHz AHB bus clock