

### General Description

This core is a universal input / output / bidirectional controller, with the width of the outputs being sizeable. The following modes of operation are available within the GERAGPIO macro.

- Reset mode
- Polling input mode
- Rising edge interrupt input mode
- Falling edge interrupt input mode
- Output mode
- AUX output mode
- Bidirectional mode.

Manual: GERA-GPIO Manual V1.1.pdf

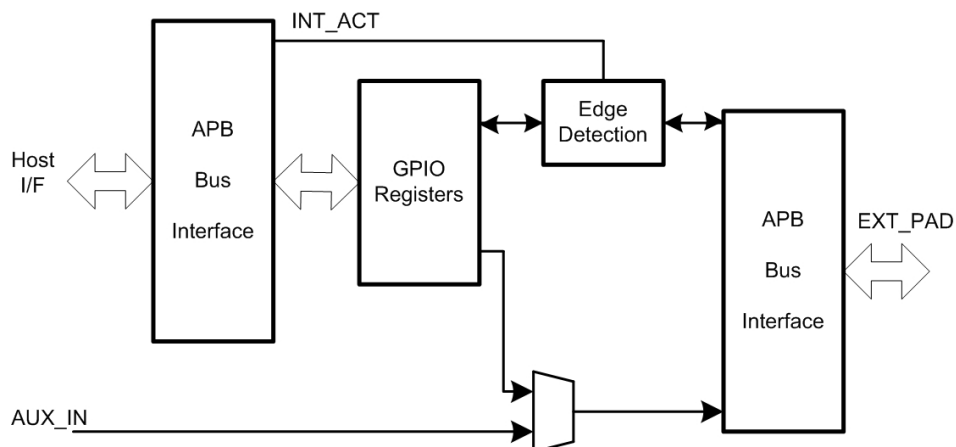
### Features

- Each pin can be used in input or output mode. Special hardware ports, which are capable of operating in three-state or open-drain mode are required to use this feature.
- AMBA 2.0 APB interface
- AMBA independent interrupt assertion line
- Pin wise controllable polling mode
- Pin wise controllable interrupt triggering on falling and rising input signal edges
- Pin wise controllable multiplexing of auxiliary inputs
- Pin wise controllable bidirectional I/O mode.

### Functional Description

The core has an AMBA APB bus communication interface and includes programmable registers that can be modified depending on the desired functionality.

### Block Diagram (one line)



### Device Utilisation & Performance

| Technology              | Device           | Utilization<br>(Average out of some different applications) | Performance              |
|-------------------------|------------------|---|--------------------------|
| Stratix III<br>(Altera) | EP3SL150F780C2   | Logic Elements: 88 (8 bit width)<br>Block Memory: 0         | 100 MHz<br>AHB bus clock |
| ArriaGX<br>(Altera)     | EP1AGX90EF1152C6 | Logic Elements: 105<br>Block Memory: 0                      | 100 MHz<br>AHB bus clock |