

General Description

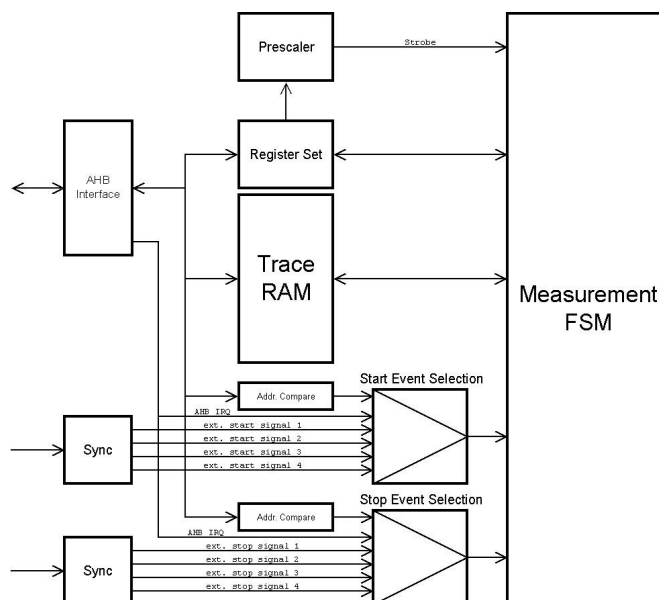
The AHB Histogram Module is used to continuously measure and record the latency and the jitter between two events. To get the latency and the jitter between two events a test setup, where the start and the stop event occurs several times sequentially, is needed. The recording can run over a long period of time (hours). After recording is finished the latency can be read out as histogram. This means the AHB Histogram Module is meant to measure a latency which is likely to jitter, like the software response of an interrupt.

Manual: GERA-HISTOGRAM_Manual V1.0.pdf

Functional Description

To record a wide range of different latencies a trace RAM and a configurable prescaler is used. Every entry of the trace RAM has a 32 bit width. The size of the trace RAM can be configured with a generic before the synthesis. By default the trace RAM has a size of 4096 entries. When the start event occurs a counter starts incrementing. When the prescaler is disabled the counter will be incremented every clock cycle. When a prescale factor of e.g. $\frac{1}{4}$ is configured the counter will only be incremented with every fourth clock cycle. This counter can also be seen as address pointer to the trace ram. That means the counter always points to one entry of the trace RAM. When the stop event occurs the trace RAM entry, which the counter is pointing at this moment, will be incremented. After that the counter will be set to zero until the next start event occurs. This means the resolution of the histogram depends on the trace RAM size, the selected prescale factor and the clock frequency.

Block Diagram



Device Utilisation & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
Stratix III (Altera)	EP3SL150F780C6	Logic Elements: 1574 Block Memory: 131.072 bit	100 MHz APB bus clock
ArriaGX (Altera)	EP1AGX90EF1152C2	Logic Elements: 1574 Block Memory: 131.072 bit	100 MHz APB bus clock