

General Description

This core stores the parameters of the design during the generation of the top VHDL netlist. This information is used by the operating system to initialize the drivers for the design.

We open the data structure if a developer wants to adapt his own OS.

Manual: no

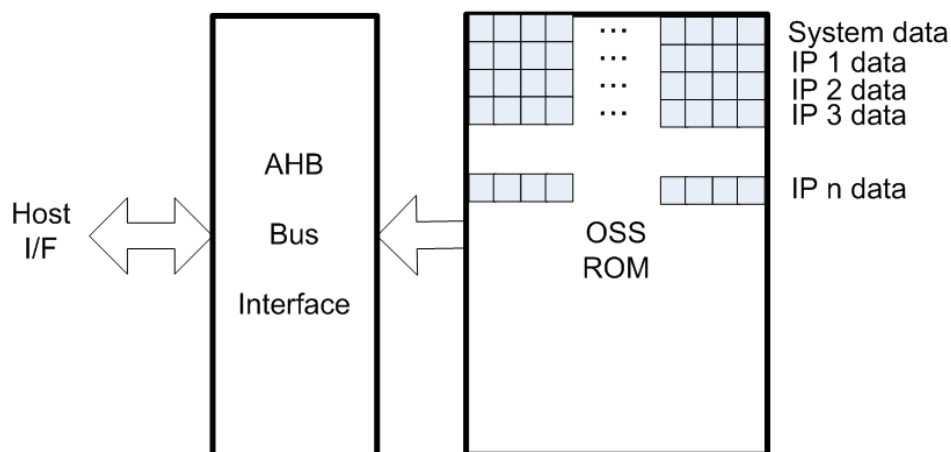
Features

- AMBA 2.0 AHB interface
- Stores the following data:
 - o IP identification
 - o System clock
 - o Interrupts
 - o Address range
 - o Generics
 - o Pinning preset

Functional Description

The core has an AMBA AHB bus communication interface.

Block Diagram



Device Utilisation & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
Stratix III (Altera)	EP3SL150F780C2	Logic Elements: 77 Block Memory: depends on numbers of IP	100 MHz AHB bus clock
ArriaGX (Altera)	EP1AGX90EF1152C6	Logic Elements: 73 Block Memory: depends on numbers of IP	100 MHz AHB bus clock