

## General Description

Gleichmann Electronics Research provides a PCI Express® core interfacing with Altera FPGAs such as Stratix II GX and Arria GX for instance. The core implements all of the required layers and features defined by the PCI Express® 1.1 specification. Additionally, interrupts (MSI as well as MSI-X) are supported.

The native Endpoint can act as a completer as well as a requester and it is recommended to use it with the additionally available AHB bridge. This low cost core is limited to one single lane.

The interrupt controller will be automatically added in the Hpe®\_AIM with the number of required interrupts. For data transmission security we add a buffer of the last 4 messages to the retry system. To reduce the RAM size this buffer can be reduced on demand,

Manual: Standard PCI Express specification

## Features

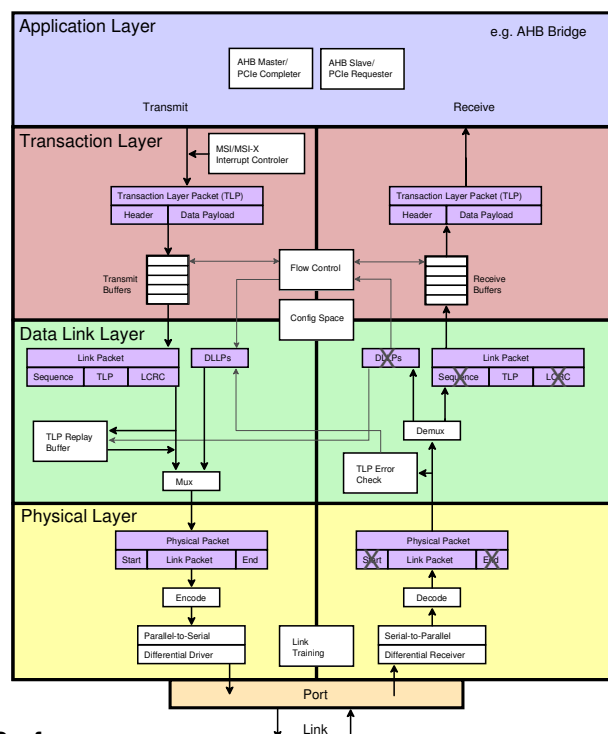
- AMBA 2.0 AHB master and slave interface
- Compatible to PCI Express® Base Specification,
- revision 1.1: Gen1 mode (2.5 Gbits/sec per direction)
- Supports Endpoint
- x1, PIPE interface to FPGA PHY: 16 bit/125 MHz
- Up to 4 Base Address Registers (BARs) available for Endpoints, 1 BAR is reserved for MSI-X configuration
- Up to 32 MSI and/or up to 2048 MSI-X interrupts are available
- AHB bridge connects the completer part to an AHB master (reachable via BAR 0) and the requester part to an AHB slave (driver has to configure the address via BAR 1)

## Functional Description

The core implements a x1 PCI Express® connection from a PCI Express® capable PC to the user's application layer. The core requires an Altera FPGA with transceiver blocks. If the driver on the PC also allows interrupts, the application layer can send them.

Intentionally, the core is used together with an AHB bridge (AHB master/slave pair) as application layer.

## Block Diagram



## Device Utilisation & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
ArriaGX (Altera)	EP1AGX90EF1152C6	Logic Elements: 13.940 Block Memory: 1.089.540 bit (Retry buffer = 4 TLP with max. payload – can be reduced)	100 MHz AHB bus clock