

General Description

This core is a free synthesizable RAM block. The minimum size is 8 Byte; the maximum size is 2 GByte. Please refer to the used FPGA technology.

Features

- AMBA 2.0 AHB slave interface
- Maximum address range up to 29 bit
- Maximum data width 32 bit
- Technology independent through RAM inference

Manual: GERA-RAM Manual V1.0.pdf

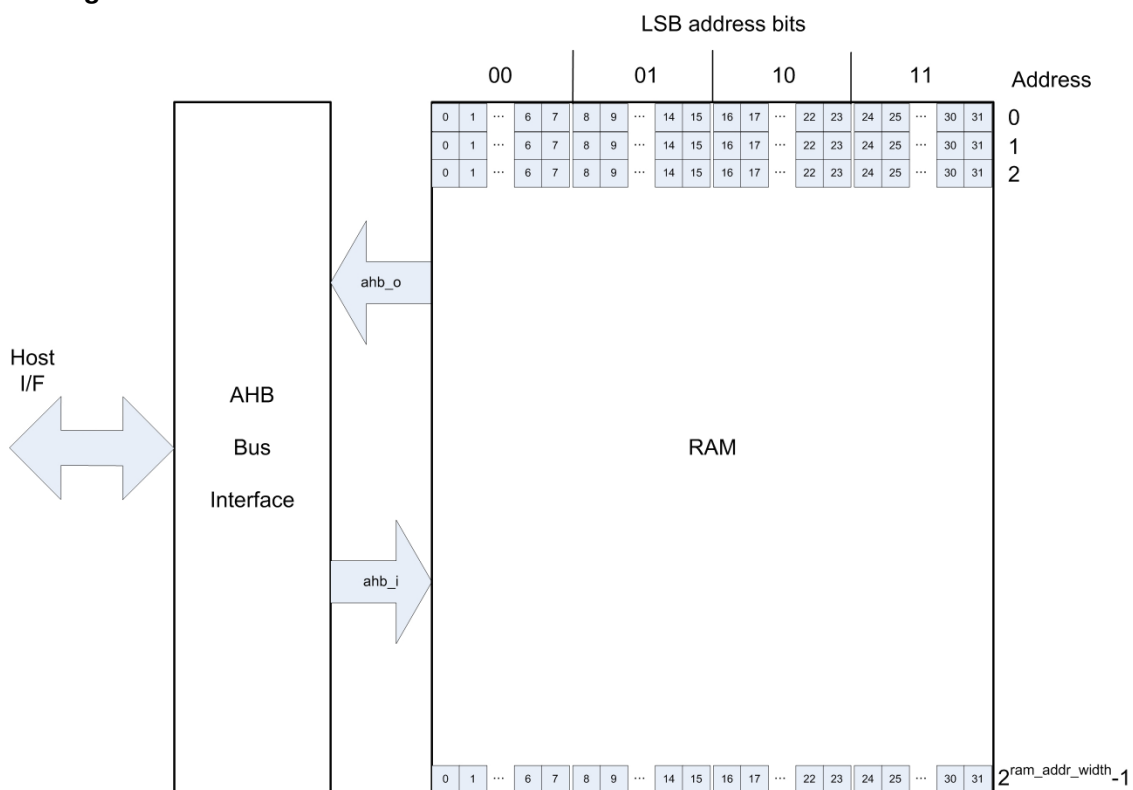
Functional Description

The core has an AMBA AHB bus communication interface. So the data bus width is 32 bit. Generally 32 bit are reserved for addressing but the lower 2 bits are reserved for byte addressing.

'00' addresses word (32 bit)

'01' addresses half word (16 bit)

Block Diagram



Device Utilisation & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
Stratix III (Altera)	EP3SL150F780C2	Logic Elements: 50 Block Memory: depends on RAM size	100 MHz AHB bus clock
ArriaGX (Altera)	EP1AGX90EF1152C6	Logic Elements: 53 Block Memory: depends on RAM size	100 MHz AHB bus clock