

General Description

This core provides serial communication capabilities, which allows communication with modem or other external devices, like another computer using a serial cable and RS232 protocol. The GERA-UART (Gleichmann Electronic Research AMBA UART) is designed to be compatible to the industry standard NS16550A (National Semiconductor UART) with the main exception that only the FIFO mode is supported and the scratch register is removed, as it serves no purpose.

Manual: GERA-UART Manual V1.0.pdf

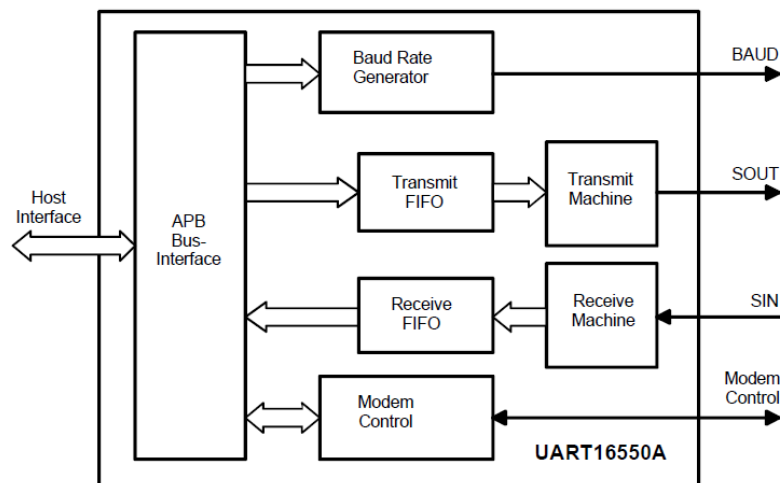
Features

- AMBA 2.0 APB interface
- Independently controlled transmit, receive, line status and data set interrupts
- Full prioritised interrupt system controls
- Configurable receiver and transmitter FIFO depth
- Programmable baud generator
- Line break generation and detection
- Fully programmable serial-interface
- Configurable additional prescaler feature and FIFO trigger level bits (126 bytes possible)

Functional Description

The core has a AMBA APB bus communication interface and includes programmable registers that can be modified depending on the desired communication protocol and communication target. Serial communication between two systems is mainly obtainable with two pins (serial in and serial out) and can optionally be extended for modem communication and handshake functionality. The core includes a prioritised interrupts system where all generated interrupts can be enabled or disabled as desired. Testbench is available and synthesis for FPGA technology has been done.

Block Diagram



Device Utilisation & Performance

Technology	Device	Utilization (Average out of some different applications)		Performance
		FIFO depth (Rx and Tx): 128 words	FIFO depth (Rx and Tx): 16 words	
Stratix III (Altera)	EP3SL150F780C6	Logic Elements: 1200 Block Memory: 2048 bit	Logic Elements: 535 Block Memory: 256 bit	100 MHz APB bus clock
ArriaGX (Altera)	EP1AGX90EF1152C2	Logic Elements: 1240 Block Memory: 2048 bit	Logic Elements: 580 Block Memory: 256 bit	100 MHz APB bus clock